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Introduction

The chip communication protocol is now provided. This manual has marked the meanings of the internal registers of the chip, which facilitates customers to directly refer to them.

1. Programming guide

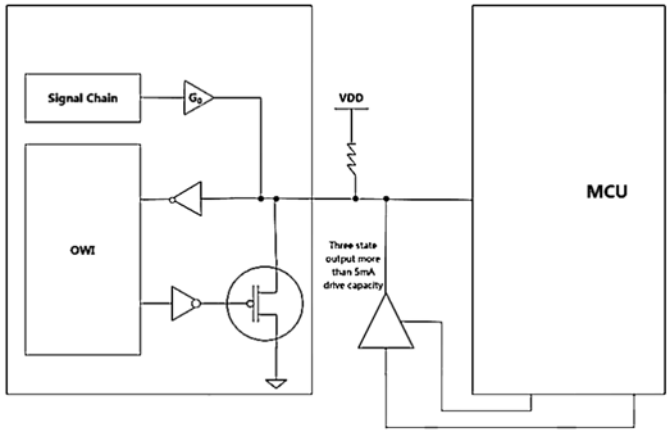

Figure 1 Schematic diagram of the OWI hardware interface

■ Power on and enter the window period of OWI (One-Wire Interface)

The GSA301 provides current-limiting output to the Vout pin for the first 20/100ms window after the end of the internal POR (Power On Reset) and allows the OWI programming interface to be activated by external circuits (this window can be programmed to close permanently, It is recommended that customers choose whether to turn off according to their own application environment).GSA301 needs power supply coordination to enter the communication.

*Note1: In this process, it is recommended that the customer use a three-state output gate with an output capacity of more than 5mA to force the Vout signal to the digital level of '0' or '1' to enable the OWI interface of the GSA301 to be activated.

■ Temporary exit of OWI communication

During the module level calibration of the current sensor, the customer can write any value to the 0x20 register to temporarily exit the OWI interface communication and restore the Go current-limiting output (current limiting to 1mA). After a waiting period(the length of which is determined by the values of the two registers 0x21 and 0x22), the GSA301 will automatically re-enter the OWI communication mode and turn off the Go output.

■ Permanent shutdown of OWI communication

In most application scenarios, the customer does not want the chip to enter the OWI mode after the factory calibration and burning NVM. If there is such a need, the customer can burn the NVM address 0x30 register value bit0 set to 1, so that after the next power-on there will be no more 20/100ms OWI window period, OWI programming interface is permanently closed. After the OWI communication is permanently turned off, the GSA301 directly outputs the analog semaphore normally 1ms after powering on the POR.

2. Register Description

■ Debugging and calibration register area

The debugging and calibration register area of GSA301 is mainly used for customers to do system calibration, debugging and control when burning NVM. The data in the debug and calibration register area will not be saved after power failure. The address space of the register area is from 0x00 to 0x12.

Table 1 Details of GSA301 debug and calibrate register area address

Address	Read and write	Name	Features	Default
0x00	W	SoftReset	Write 0x24 to this register, software reset chip	0x00
0x01~0x05	NA	NA	NA	NA
0x06	R	TADC_H	12-bit TADC current conversion value data 4 bits higher (Bit7~4 are all zeros)	0x00
0x08	RW	ZeroDAC_H	14 bit zero bias fine-tune register high 6 bits with calibration mode not enabled, read only, the value is the value of the current ZeroDAC control word. When calibrating mode is enabled (see Register 0x10), writing this register immediately changes the ZeroDAC control word and acts as an output.	0x00
0x09	RW	ZeroDAC_L	14 bit zero bias fine tune register 8 bits lower Calibration mode not enabled, read only, value is the value of the control word of the current ZeroDAC When calibrating mode is enabled (see Register 0x10), writing this register immediately changes the ZeroDAC control word and acts as an output.	0x00
0x0A	RW	GainDAC_H	14 bit gain fine-tuned register High 6 bits When calibrating mode is not enabled, read only, the value is the value of the current GainDAC control word When calibrating mode is enabled (see register 0x10), writing this register immediately changes the GainDAC control word and acts as an output.	0x00
0x0B	RW	GainDAC_L	14 bit gain fine-tuned register Low 8 bits When calibrating mode is not enabled, read only, the value is the value of the current GainDAC control word When calibrating mode is enabled (see register 0x10), writing this register immediately changes the GainDAC control word and is used for output.	0x00
0x0C~0x0F	NA	NA	NA	NA
0x10	RW	Calib_Mode	Bit0: Calibration mode enabled	0x00

			● Set 0- Without using calibration mode, the value of register 0x08 to 0B is the GainDAC and ZeroDAC values written to the response register after calibration. ● Set 1- activates calibration mode, allowing registers 0x08~0B to be written。	
0x12	RW	Blow_Start	Bit1:Blow_Start ● Set 1- start burn write NVM (customers need to wait in the software for some time before doing other read and write operations).	0x00

■ NVM Global Control Variable area

The global control variable area of GSA301 is primarily used to control options that are not relevant for customer and system calibration. In general, this area saves the settings without the need for secondary programming.

Table 2 Details of GSA301 NVM global control variable area address

Address	Read and write	Name	Features	Comments
0x30	RW Blow	Sys_Config	● Bit7: MTP_EN set 0: NVM customer calibration parameter area using OTP mode (when OTP mode is used, Bank1 data and corresponding Bank2 data are done or logical as the actual configuration value). set 1: NVM customer calibration parameter area uses MTP mode (When using MTP mode, customer uses Bit6 of register 0x30 to select Bank1 data or a set of Bank2 data as the actual configuration value). Only when set to MTP mode can you burn 3 times. ● Bit6:CONFIG_MTP_SEL (works only in MTP mode) set 0: ConfigBank1 data, Bank1 points to register 0x40/0x41 set 1: ConfigBank2 data, Bank2 points to register 0x42/0x43 ● Bit5: Set to 1 ● Bit4~1: **One programming:** LUT_TABLE_BANK_SEL <3:0> 0001b: use the data in LUTBank1 as the power-on default values for GainDAC and ZeroDAC, as well as the	

			block for fixed output. **Secondary programming:** LUT_TABLE_BANK_SEL <3:0> 0011b: use the data in LUTBank3 as the power-on default values for GainDAC and ZeroDAC, as well as the block for fixed output. **Tertiary programming:** LUT_TABLE_BANK_SEL <3:0> 0111b: use the data in LUTBank7 as the power-on default values for GainDAC and ZeroDAC, as well as the block for fixed output. ● Bit0: OWI_Disable set 0: The OWI interface is not disabled. set 1: The OWI interface is permanently disabled, and there is no 20/100ms window after it is started again.	
0x31	RW Blow	Sys_Config _BACKUP	● Bit7~4: EXC Config 0000b: current drive 1.5mA (used on 3.3V power supply) 0010b: current drive 2.5mA (5V power supply, operating temperature is higher than 105℃ for use) 0011b: current drive 3mA (5V power supply, operating temperature is lower than 105℃ for use) ● Bit3: VEXC_SEL set 1: 2.5V (3.3V power supply) ● Bit2: INPUT_SWAP set 0: the input positive and negative are not exchanged. ● Bit1~0: SPIN_CHIP 10b : enables the self-stabilized zero function.	
0x32	RW Blow	CSTCTrim1	Bit6~0：IEXC_TC1<6:0>	TC1 values between 0 and 63
0x33	RW Blow	CSTCTrim1	Bit5~0：IEXC_TC2<5:0>	

■ NVM customer calibration parameter area

The NVM customer calibration parameter area of GSA301 is divided into Block1 and Block2 data pieces.

1) In OTP mode, the two pieces of data backup each other, and the final output value is the calculation result of the corresponding data "or" of Block1 and Block2.

2) In MTP mode, the customer can choose one of the data of Block1 or Block2 as the final output result. The data for Block1 starts from address 0x40 to 0x41, and the data for Block2 starts from addresses 0x42 to 0x43.

Table 3 Detailed description of GSA301 NVM customer calibration parameter area address

Address	Read and write	Name	Feature	Comments
0x40	RW Blow	GAIN Setting	● Bit7~6: Go gain configuration 00b: 2.4x 01b: 2.8x 10b: 3.2x 11b: 3.6x ● Bit5~3: G2 gain configuration 000b: 1.182x 001b: 1.4x 010b: 1.667x 011b: 2x 100b: 2.429x 101b: 3x 110b: 3.5x 111b: 4x ● Bit2~0: G1 gain configuration 000b:1x 001b:2x 010b:4x 011b:8x 100b:16x 101b:32x 110b:64x 111b:128x	MTPBank1
0x41	RW Blow	EXC Config& Input Option	● Bit0: output mode set 0: fixed output, gain does not change with power supply set 1: proportional output, gain changes with power supply ● Bit2~1: Vbias/V0 control 00b: Vbias output is 2.5V 01b: Vbias output is 1.65V 10b: Vbias output is 0.5V When set to 00b/01b/10b, both zero and reference voltage are fixed outputs. 11b:Vbias/V0 output 1/2VCC When set to 11b both zero and	MTPBank1

			reference voltage are proportional outputs. ● Bit3~4: Low pass filter frequency selection 00b: Not recommended 01b: 500kHz 10b: 250kHz 11b: 50kHz ● Bit7~5: NA	
0x42	RW Blow	GAIN Setting	● Bit7~6: Go gain configuration 00b: 2.4x 01b: 2.8x 10b: 3.2x 11b: 3.6x ● Bit5~3: G2 gain configuration 000b: 1.182x 001b: 1.4x 010b: 1.667x 011b: 2x 100b: 2.429x 101b: 3x 110b: 3.5x 111b: 4x ● Bit2~0: G1 gain configuration 000b:1x 001b:2x 010b:4x 011b:8x 100b:16x	MTPBank2

			101b:32x 110b:64x 111b:128x	
0x43	RW Blow	EXC Config& Input Option	● Bit0: output mode set 0: fixed output, gain does not change with power supply set 1: proportional output, gain changes with power supply ● Bit2~1: Vbias/V0 control 00b: Vbias output is 2.5V 01b: Vbias output is 1.65V 10b: Vbias output is 0.5V When set to 00b/01b/10b, both zero and reference voltage are fixed outputs. 11b:Vbias/V0 output 1/2VCC When set to 11b both zero and reference voltage are proportional outputs. ● Bit3~4: Low pass filter frequency selection 00b: Not recommended 01b: 500kHz 10b: 250kHz	MTP Bank2

			11b: 50kHz ● Bit7~5: NA	

Table 4 GSA301 3 times programming data storage location

Address	Read and write	Name	Feature	Comments
0x60 ~ 0x64	RW Blow	Room temperature point: 12bit temperature value, 14bit ZeroDAC control word, 14bit GainDAC control word	TADC⟨11:4⟩ TADC⟨3:0⟩ | ZeroDAC⟨13:10⟩ ZeroDAC⟨9:2⟩ ZeroDAC⟨1:0⟩ | GainDAC⟨13:8⟩ GainDAC⟨7:0⟩	One programming write: LUT - BANK1
0x70 ~ 0x74	RW Blow	Room temperature point: 12bit temperature value, 14bit ZeroDAC control word, 14bit GainDAC control word	TADC⟨11:4⟩ TADC⟨3:0⟩ | ZeroDAC⟨13:10⟩ ZeroDAC⟨9:2⟩ ZeroDAC⟨1:0⟩ | GainDAC⟨13:8⟩ GainDAC⟨7:0⟩	Secondary programming write: LUT -- BANK3
0x85 ~ 0x89	RW Blow	Room temperature point: 12bit temperature value, 14bit ZeroDAC control word, 14bit GainDAC control word	TADC⟨11:4⟩ TADC⟨3:0⟩ | ZeroDAC⟨13:10⟩ ZeroDAC⟨9:2⟩ ZeroDAC⟨1:0⟩ | GainDAC⟨13:8⟩ GainDAC⟨7:0⟩	Tertiary programming: write: LUT -- BANK7

Chip read/write timing instructions

a)Read: Enter the calibration mode after communication, issue the read command, and after about 1ms, the chip Vout foot will output the signal corresponding to the read command;

b)Write: After writing the register value, assign any value to the register 0x20, the chip can briefly exit the communication, and the Vout foot has a stable output voltage after about 0.1s.

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